



## Automated SmartNIC Offloading Insights for Network Functions

Yiming Qiu, Jiarong Xing, Kuo-Feng Hsu, Qiao Kang, Ming Liu, Srinivas Narayana, Ang Chen









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#### SmartNICs are very different!



Heterogeneous compute engines (e.g., SoC cores, ASIC accelerators)



Lightweight runtime (e.g., no full OS or libc support)

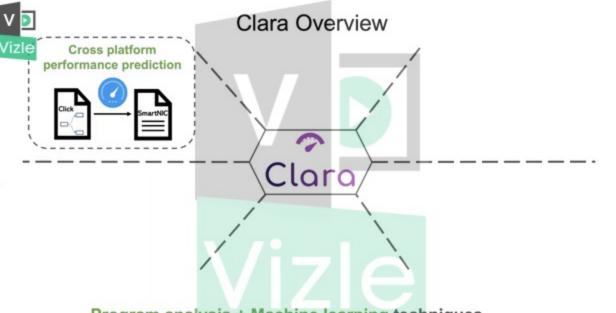


Proprietary, closed-source compiler toolchains (e.g., NFCC)



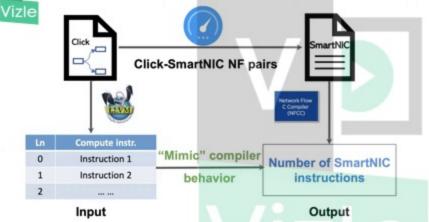
Constrained programming models (e.g., microC)

Good program performance requires expert knowledge



Program analysis + Machine learning techniques

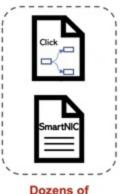




- Clara takes inspiration from Natural Language Processing
  - Learn from Click-SmartNIC pairs in their compiled forms
  - Predict by mimicking SmartNIC compiler behavior



#### Performance prediction: Data generation



Lack of ML training data!

Dozens of Legacy NF pairs

- Lack of real world Click-SmartNIC program pairs
  - Adapt program generator as data synthesizer
  - Random but representative program generation

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#### Evaluation setup

- Clara prototype
  - 7400 LoC
  - Extends YarpGen for data synthesis
  - Tensorflow, Scikit-learn, TPOT for ML
- A range of legacy network functions
  - Click modular router elements and confs
- SmartNIC platform
  - Netronome Agilio CX SmartNIC
  - Compilation in bare-metal mode (Micro C)



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